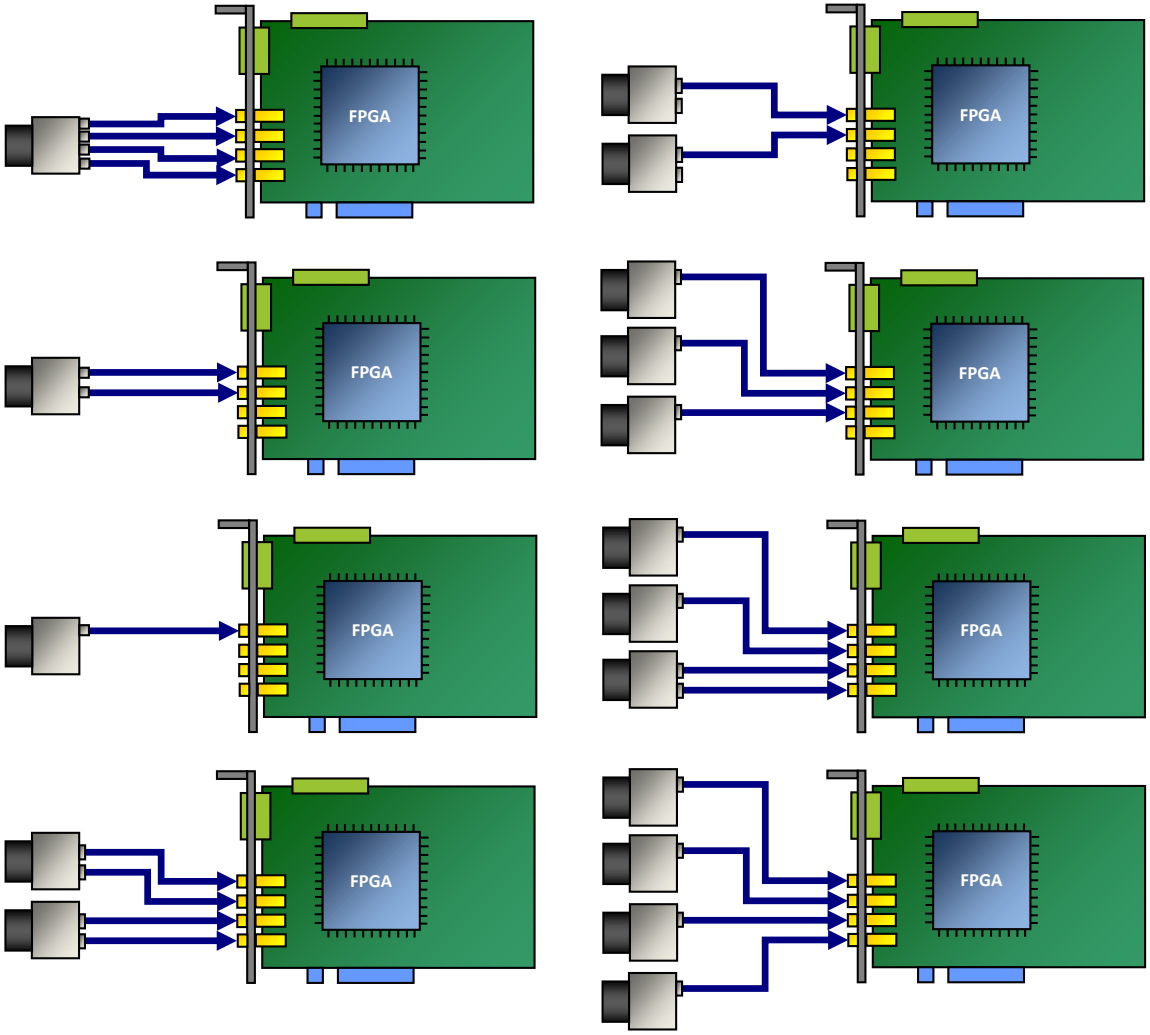
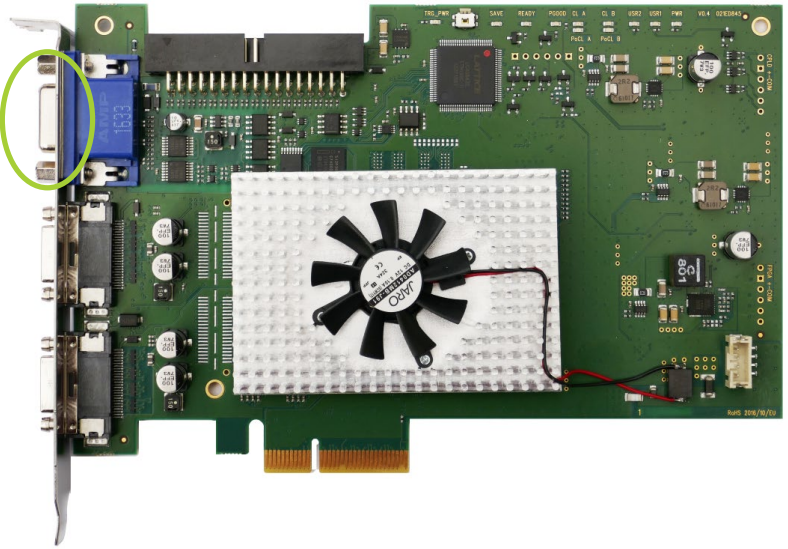
imaWorx Topology



VCLx

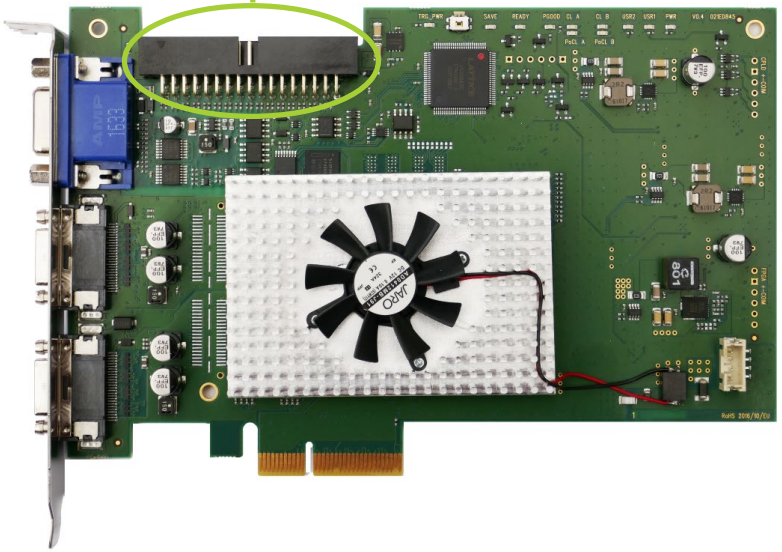
Front GPIO

Opto-coupled inputs,
TTL outputs

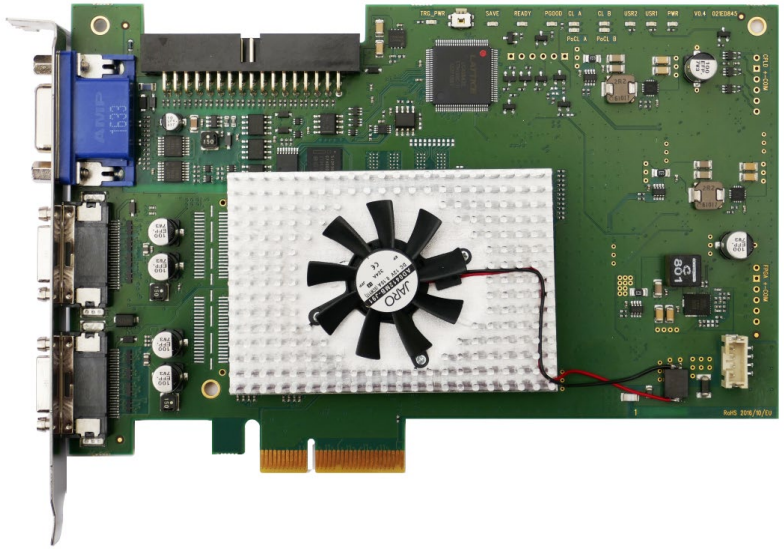


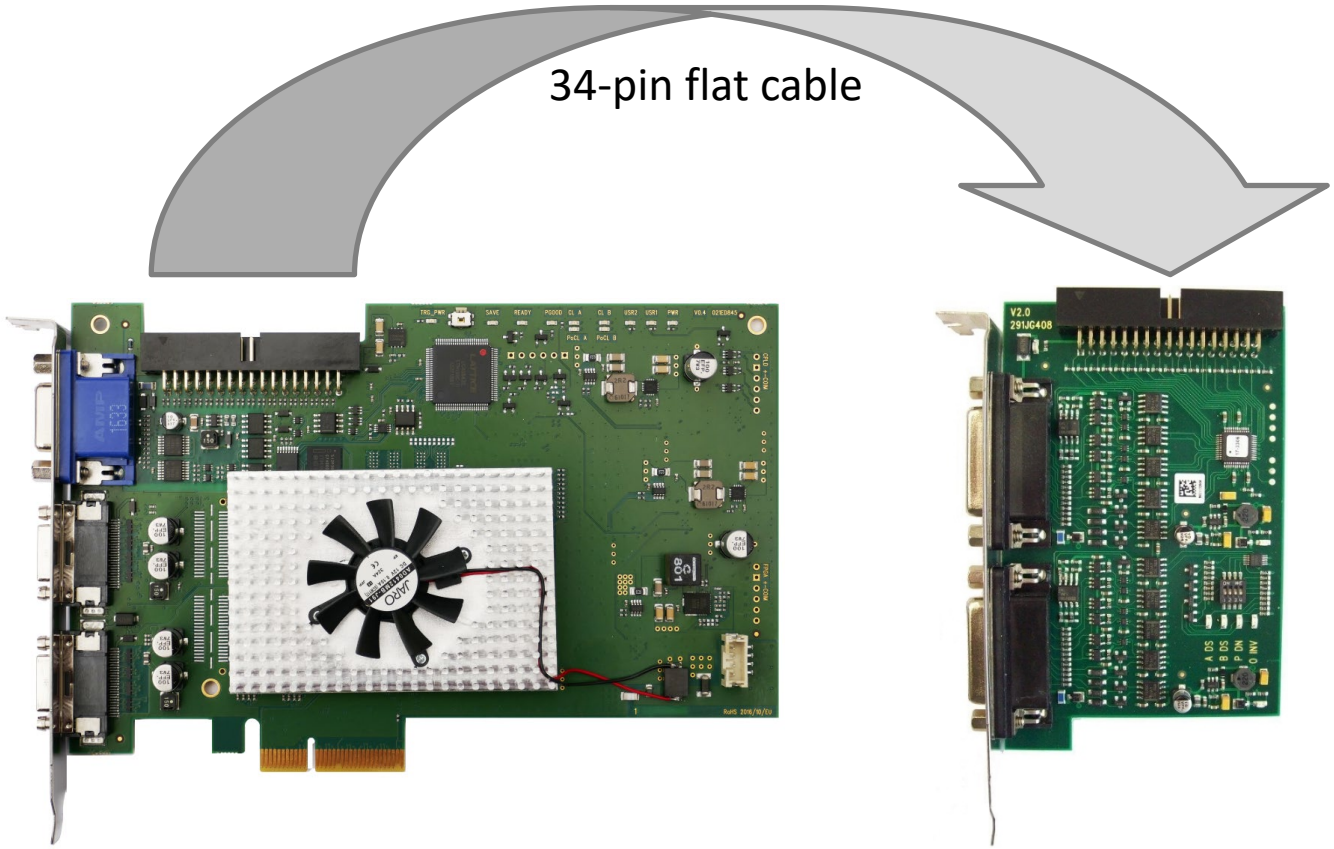
GPIO

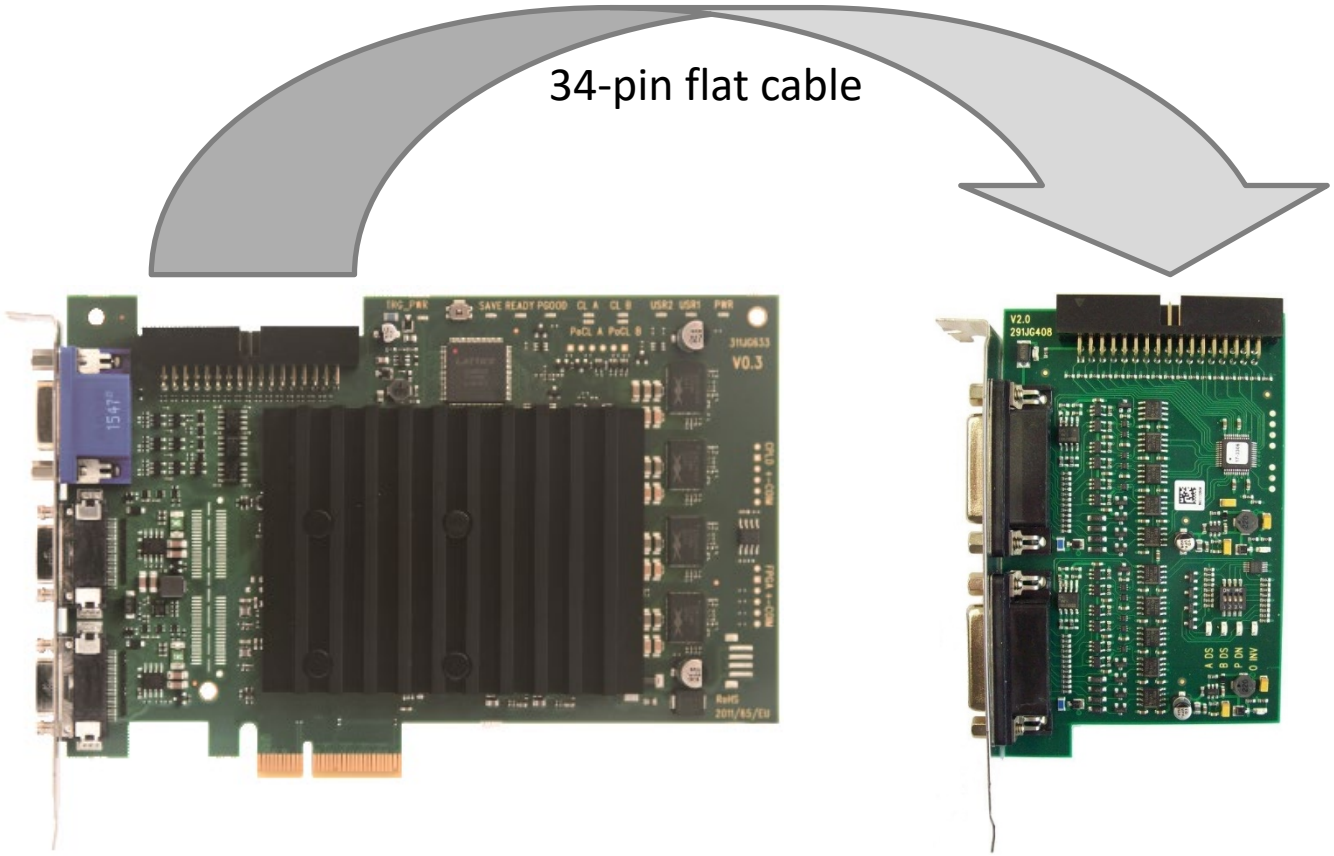
Trigger
board connection

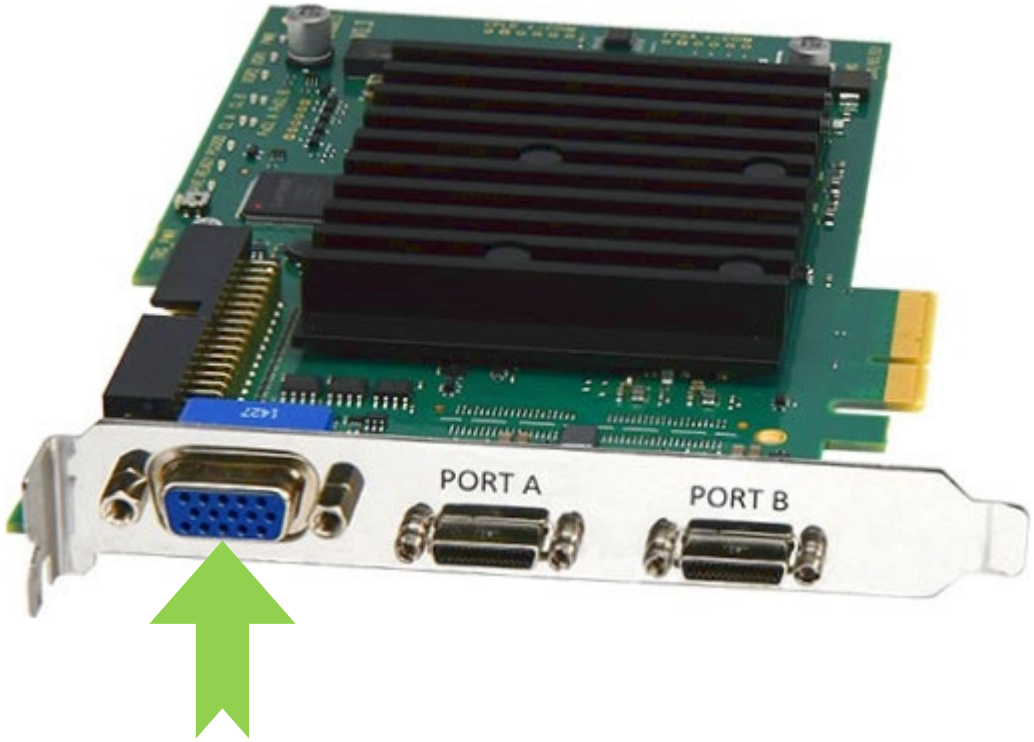


VCLx

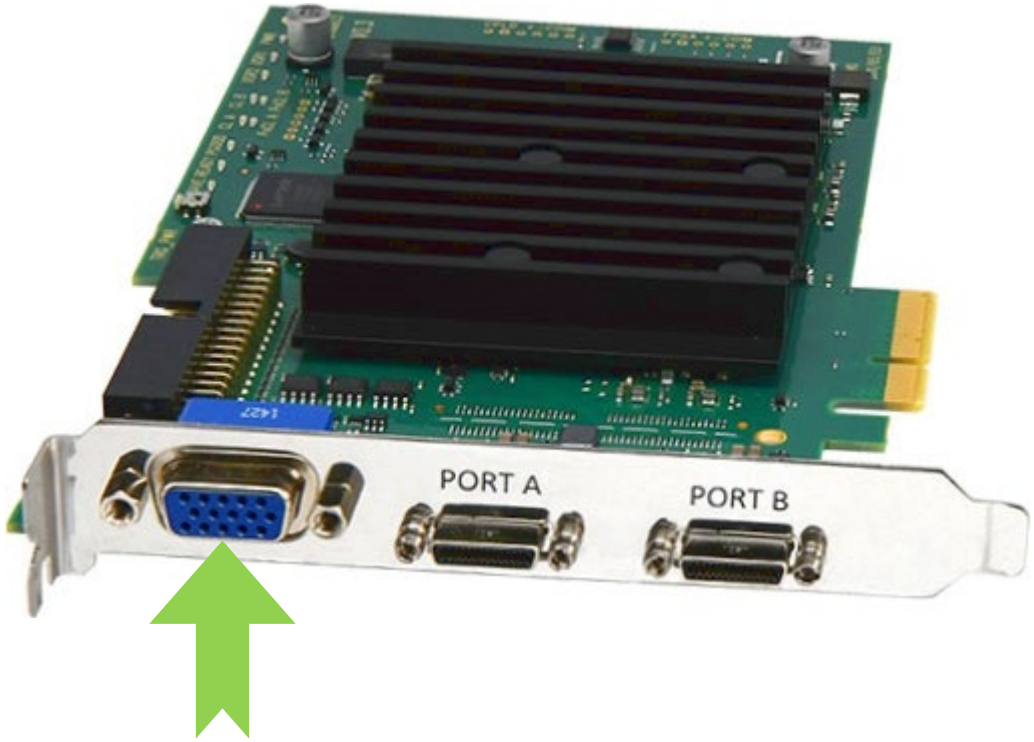



34-pin flat cable


34-pin flat cable
V0.3
V2.0



15-pin D-sub socket (Front GPIO) for triggering and synchronizing peripheral devices, including two TTO GPOs



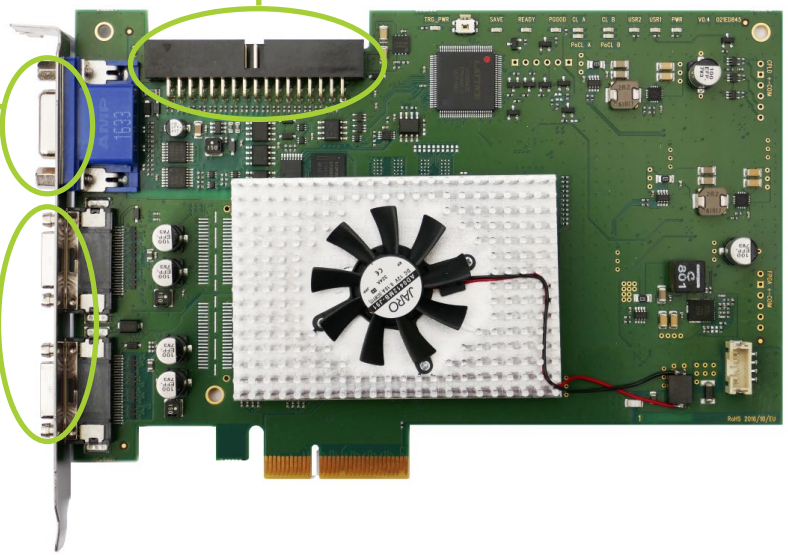
Front GPIO for triggering and synchronizing peripheral devices

VCLx

GPIO
Trigger
board connection

Front GPIO
Opto-coupled inputs,
TTL outputs

Camera Interfaces
SDR 26

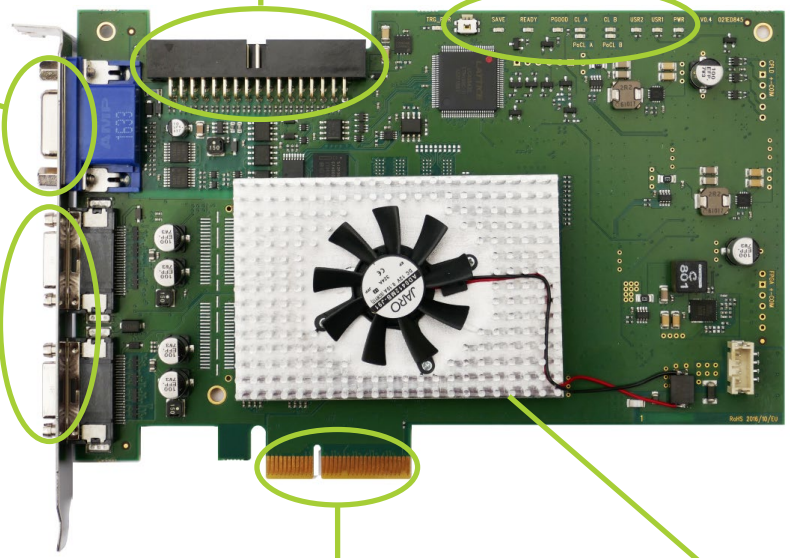


VCLx

GPIO
Trigger
board connection

LEDs & Switch

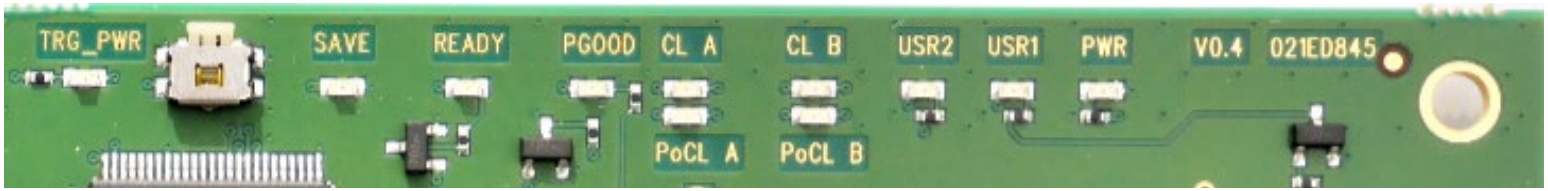
Front GPIO
Opto-coupled inputs,
TTL outputs



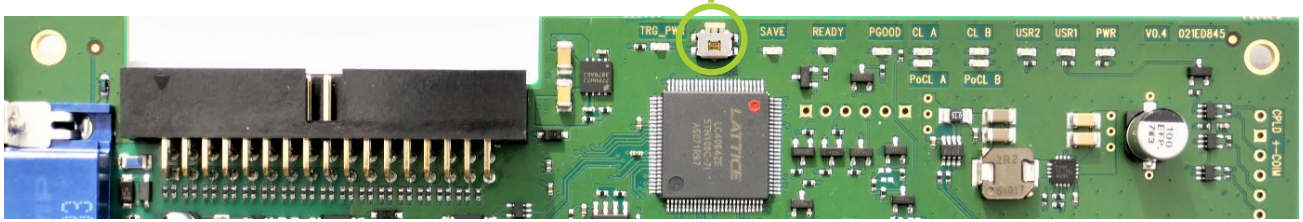
Camera Interfaces
SDR 26

DMA1800 (PCIe x4 Gen2):
Up to 1.800 MByte/s

On-board image and signal processing
(trigger and synchronisation)
on FPGA located under cooling unit

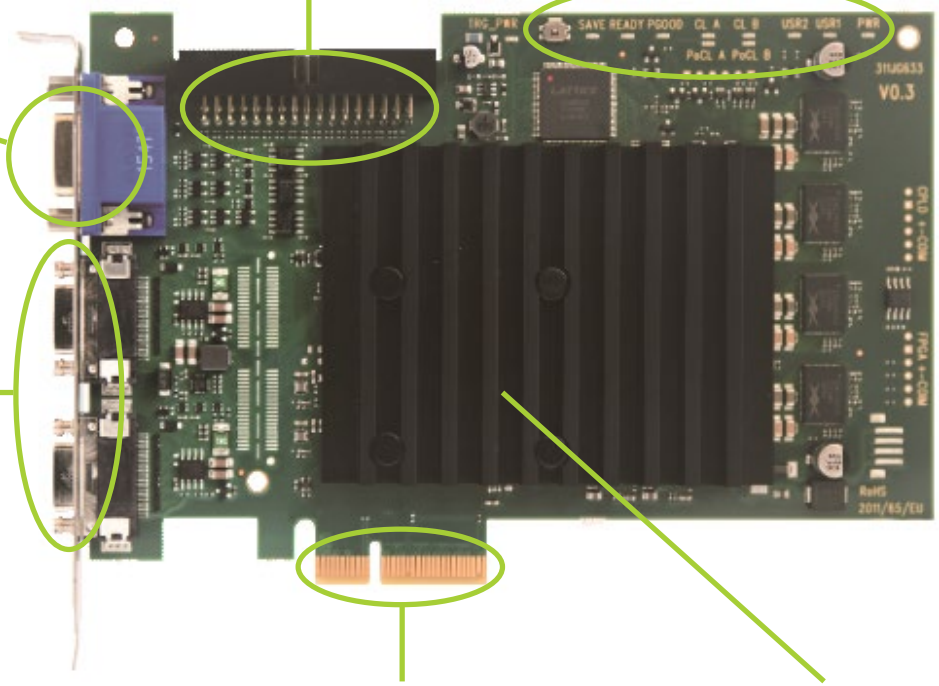


Configuration Switch





ACL/VCL



GPIO
Trigger
board connection

LEDs & Switch

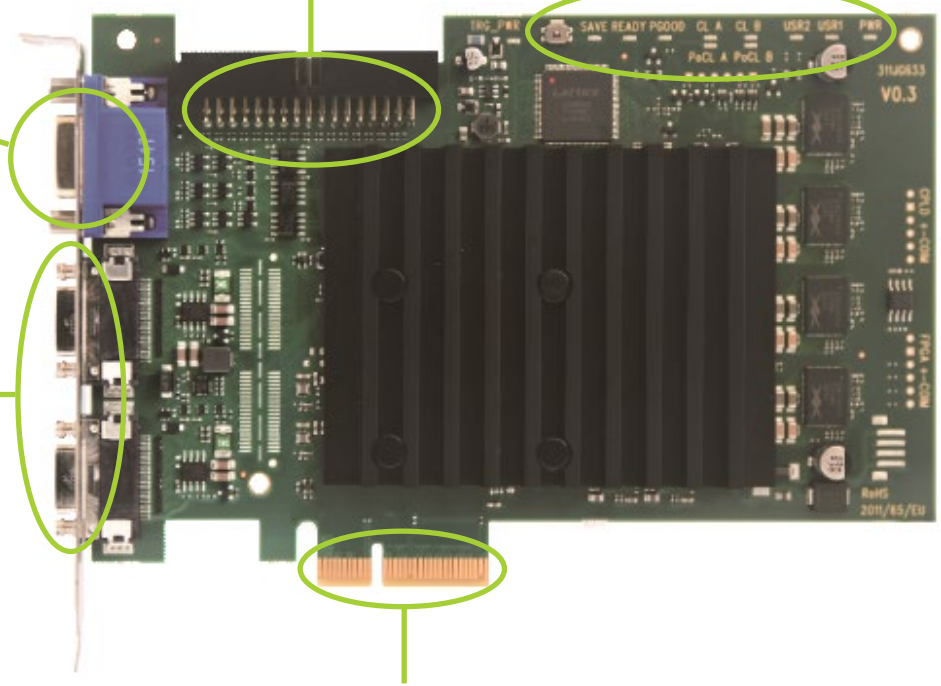
Front GPIO
Opto-coupled inputs,
TTL outputs

Camera Interfaces
SDR 26

DMA1800 (PCIe Gen2 x4):
Up to 1.800 MByte/s

On-board image and signal processing
(trigger and synchronisation)
Xilinx Kintex 7 FPGA Technology,
512 MByte DDR3 SDRAM

ACL/VCL Ports/LEDs

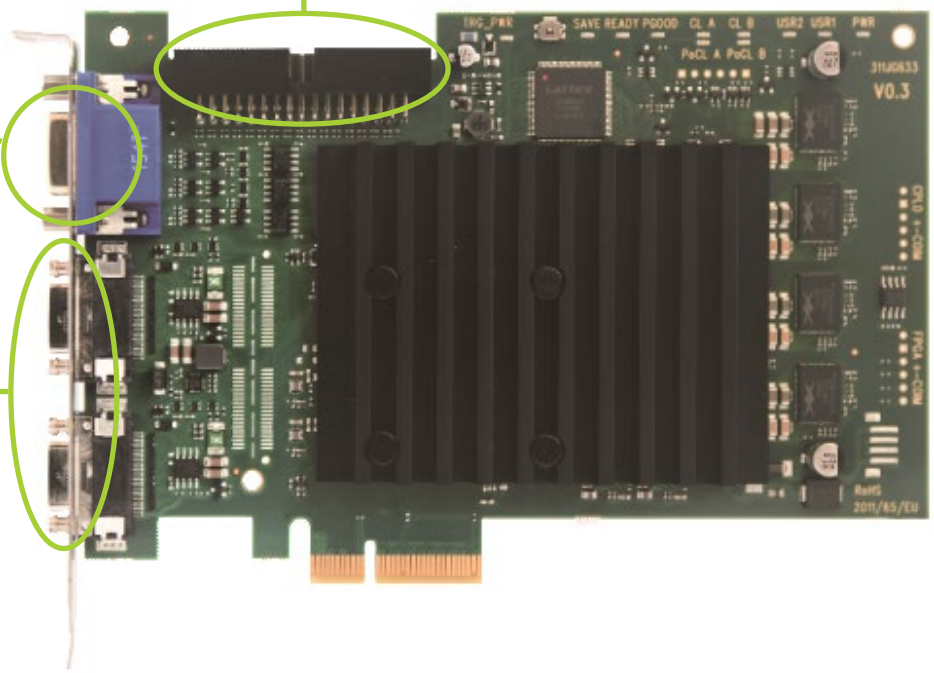


ACL/VCL Trigger Interfaces

GPIO
Trigger
board connection

Front GPIO
Opto-coupled inputs,
TTL outputs

Camera Interfaces
SDR 26



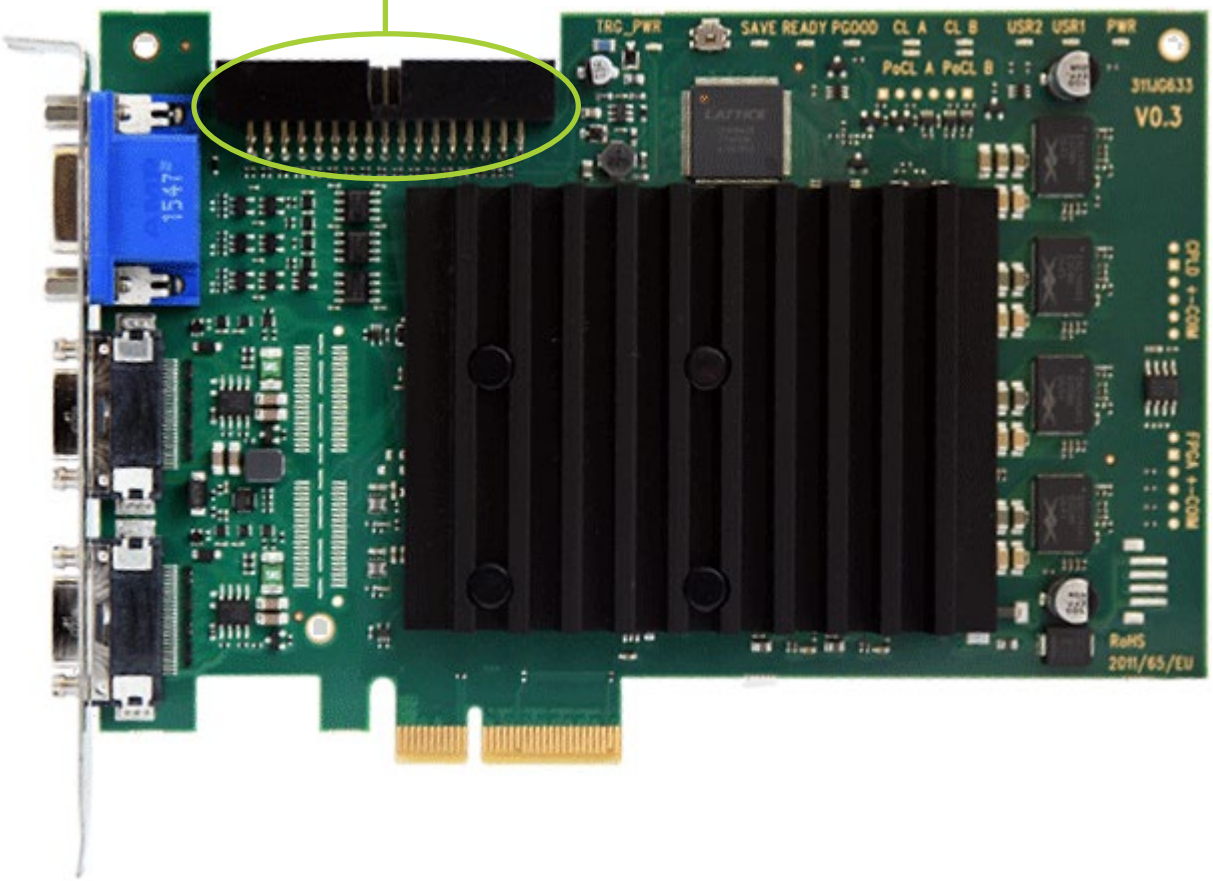
ACL/VCL


TRG_PWR
SAVE READY PGOOD CL A CL B USR2 USR1 PWR
PoCL A PoCL B
V0.3
RoHS
2011/65/EU

ACL/VCL

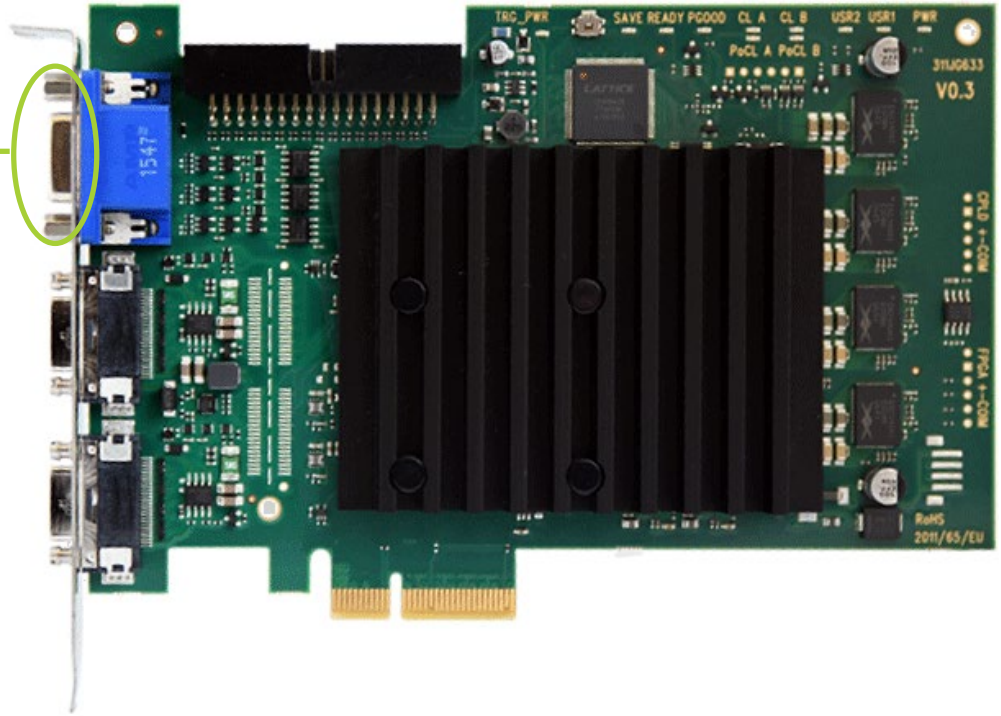
GPIO

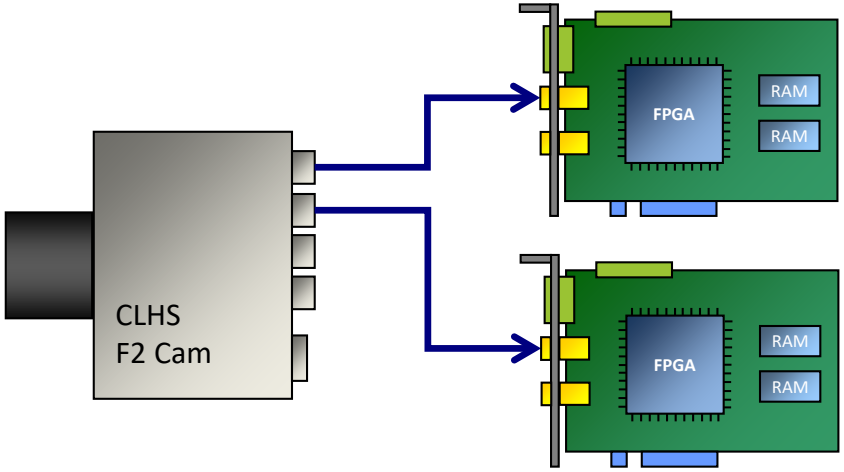
Trigger board connection

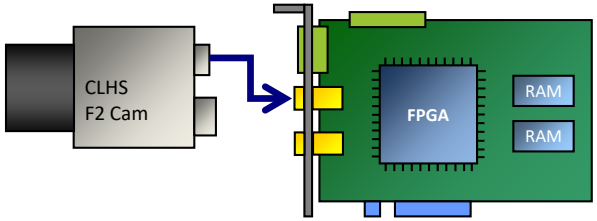


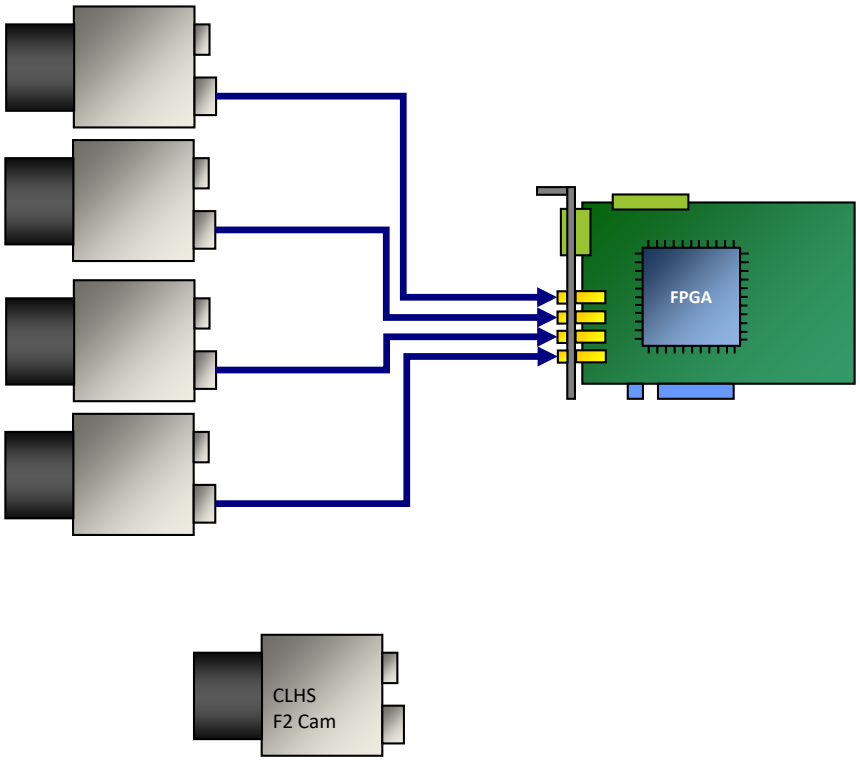
ACL/VCL

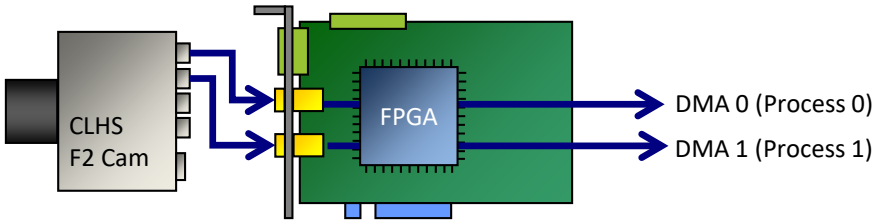
Front GPIO
Opto-coupled inputs,
TTL outputs

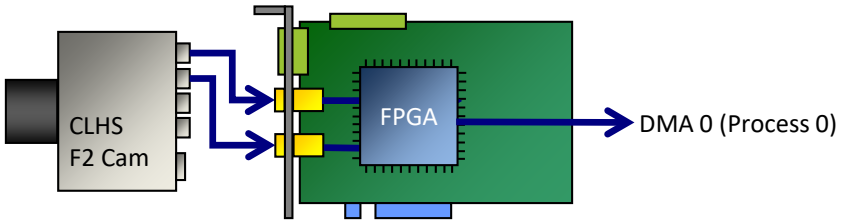


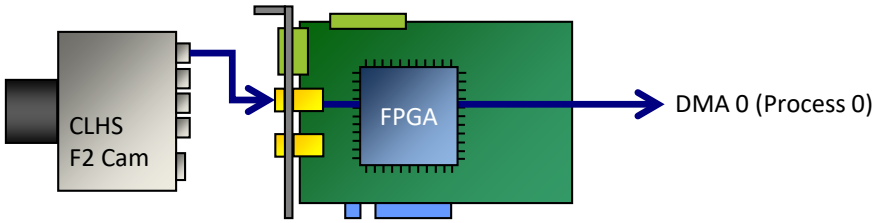

CLHS
F2 Cam
FPGA
RAM
RAM
FPGA
RAM
RAM


CLHS
F2 Cam
FPGA
RAM
RAM

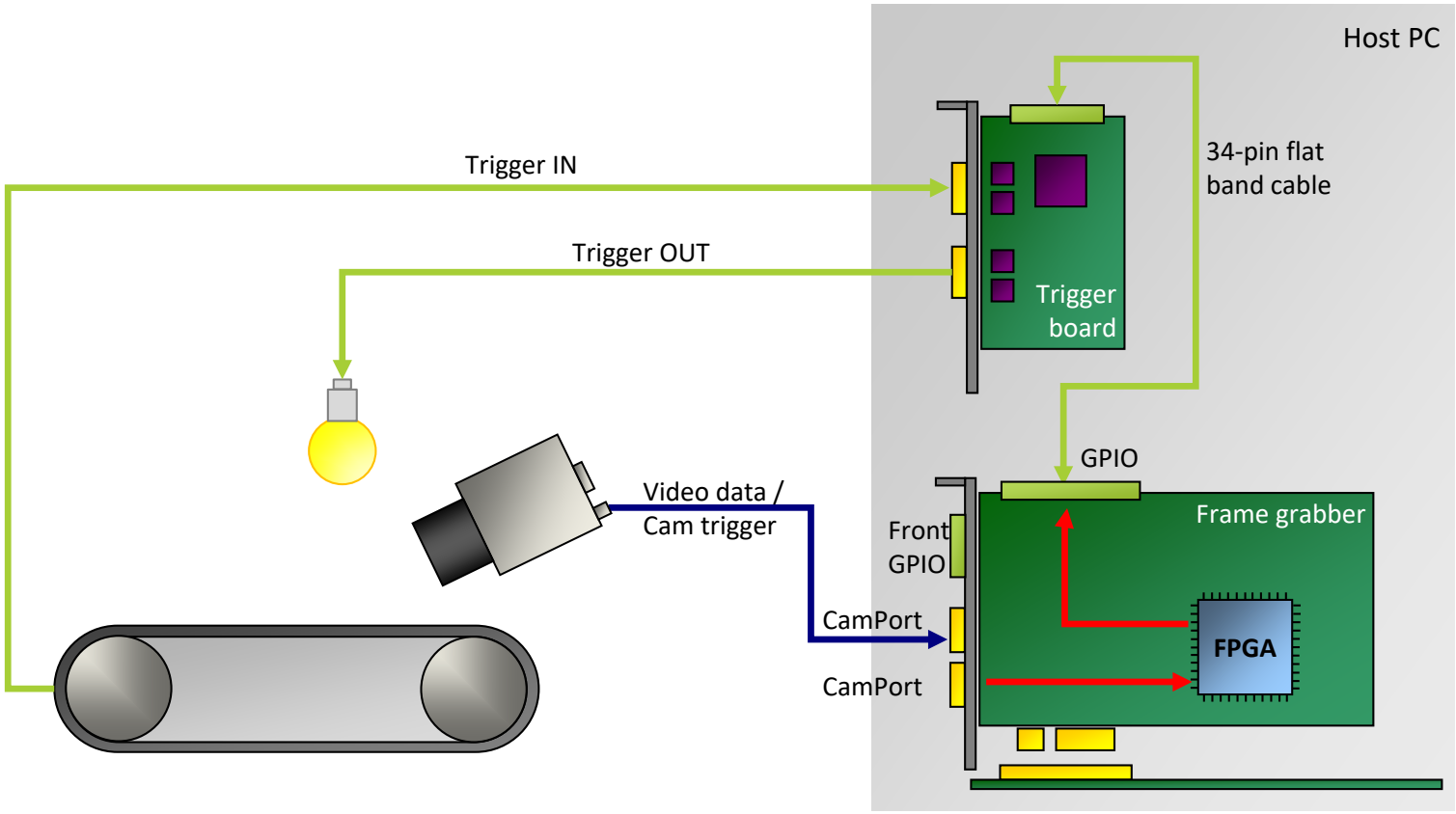

FPGA
CLHS
F2 Cam


CLHS
F2 Cam
FPGA
DMA 0 (Process 0)
DMA 1 (Process 1)

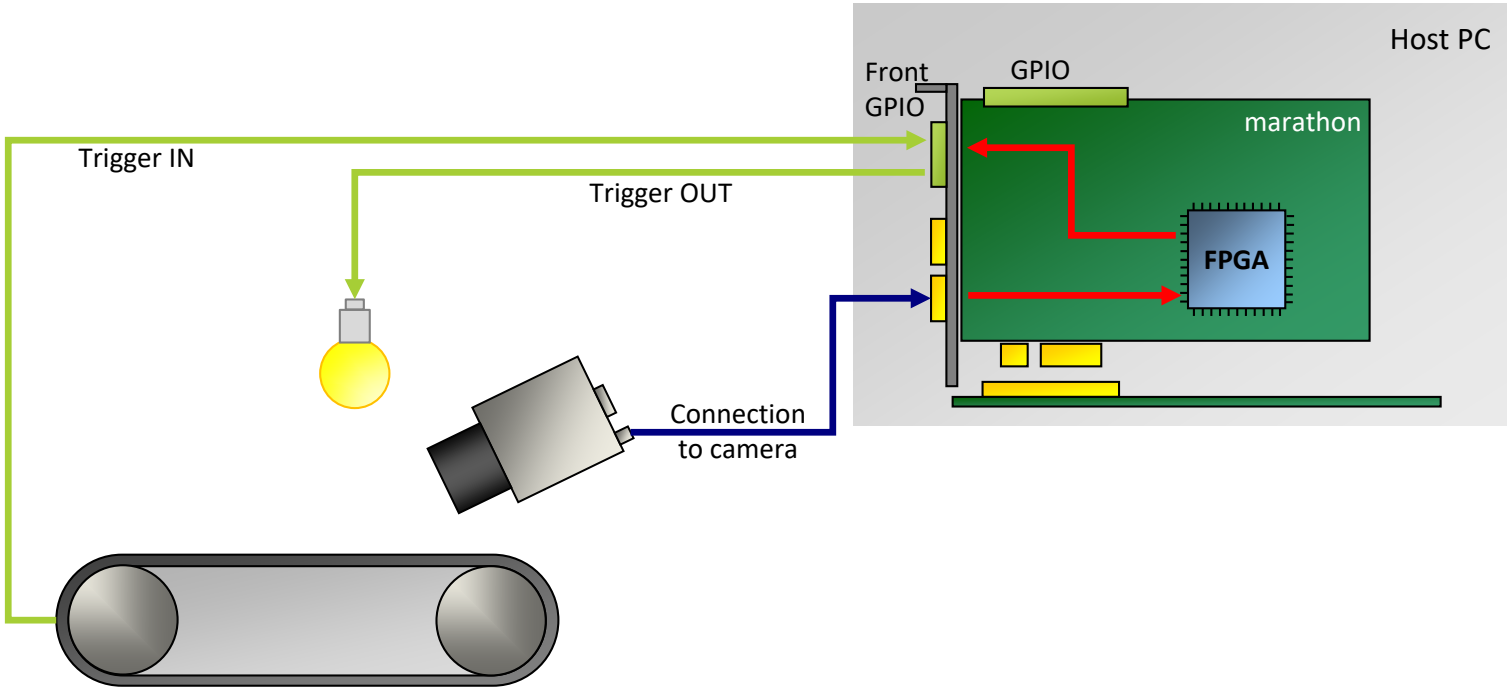

CLHS
F2 Cam
FPGA
DMA 0 (Process 0)


CLHS
F2 Cam
FPGA
DMA 0 (Process 0)

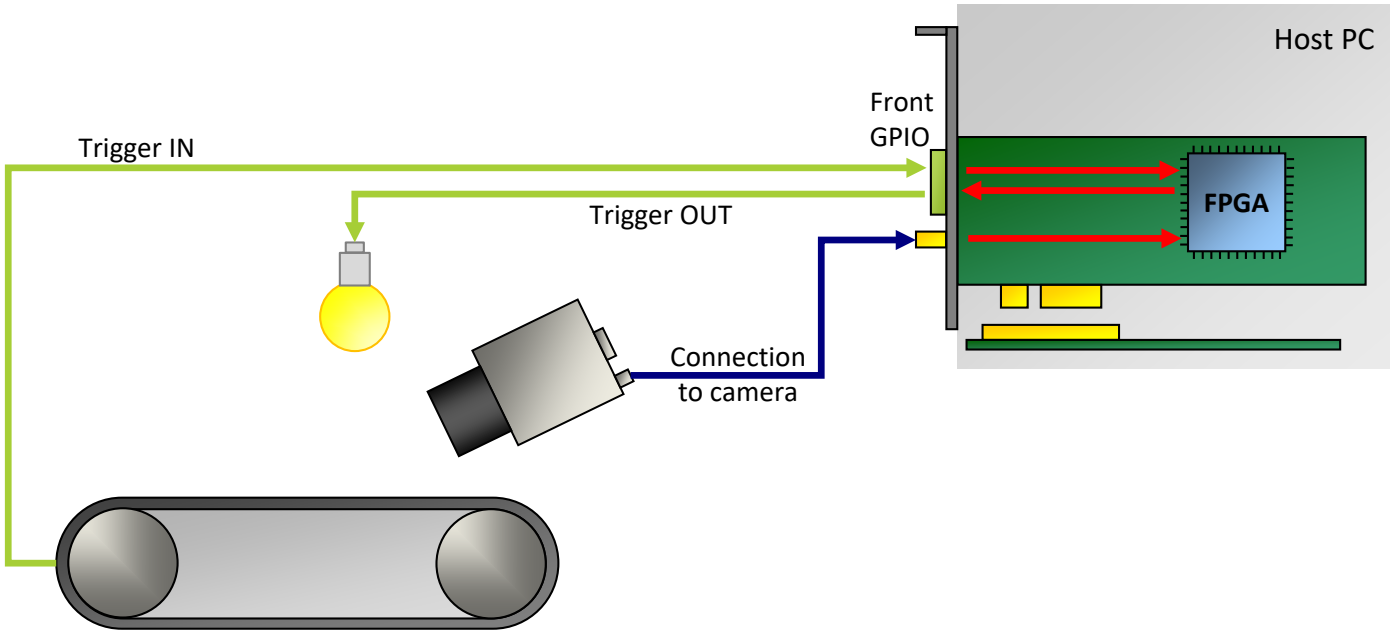
Trigger GPIO (CLHS)

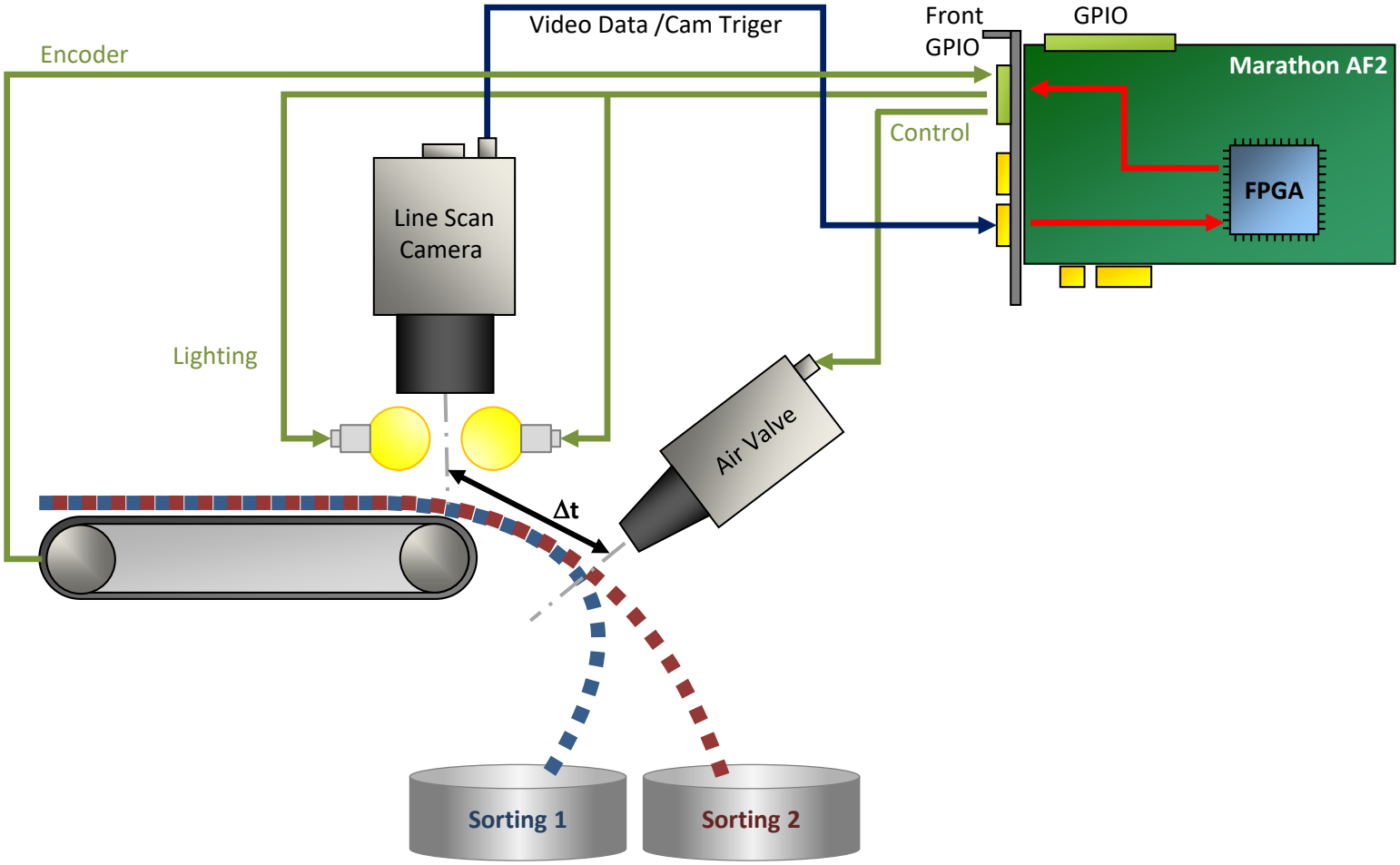


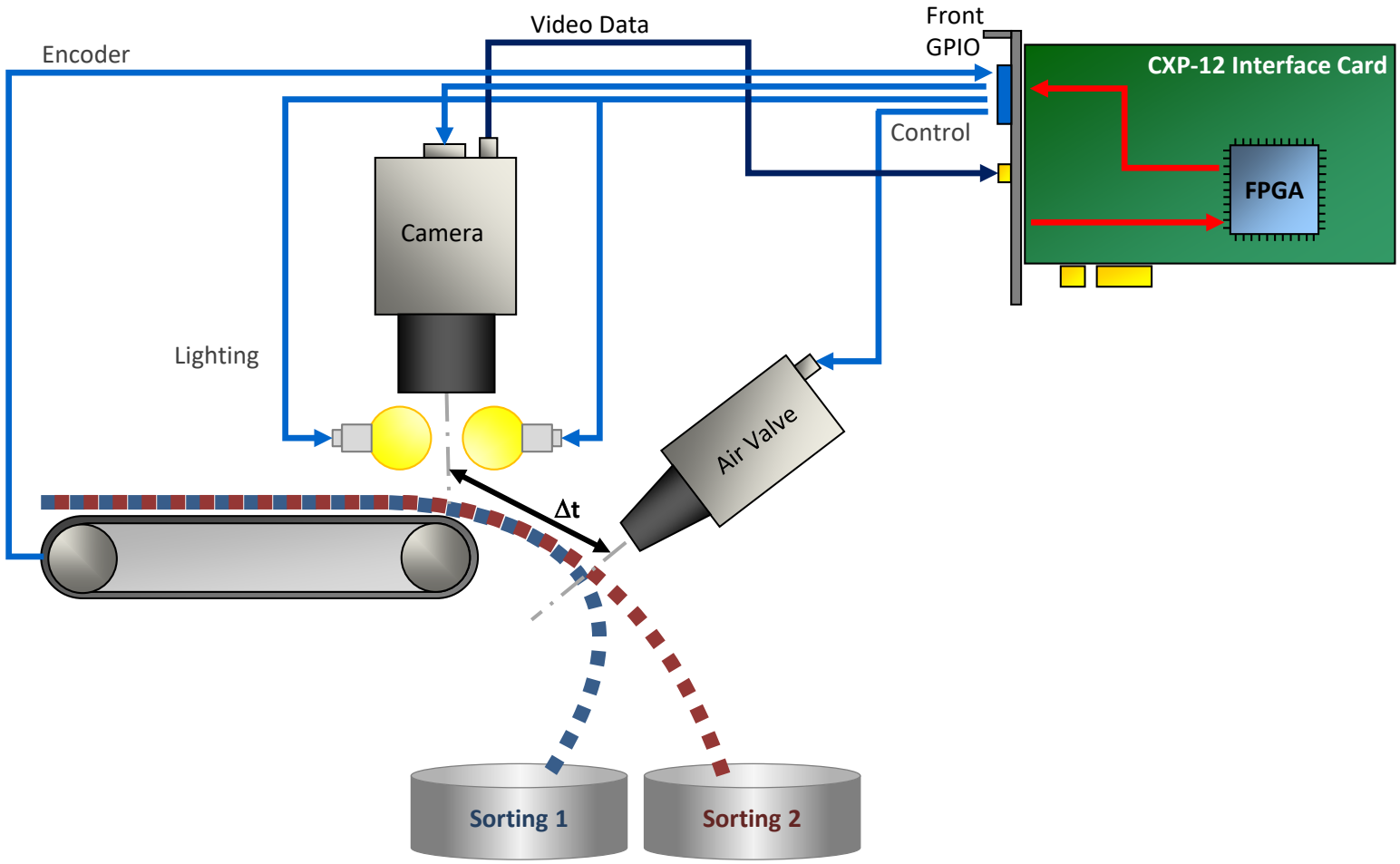
Trigger Front GPIO (CLHS)



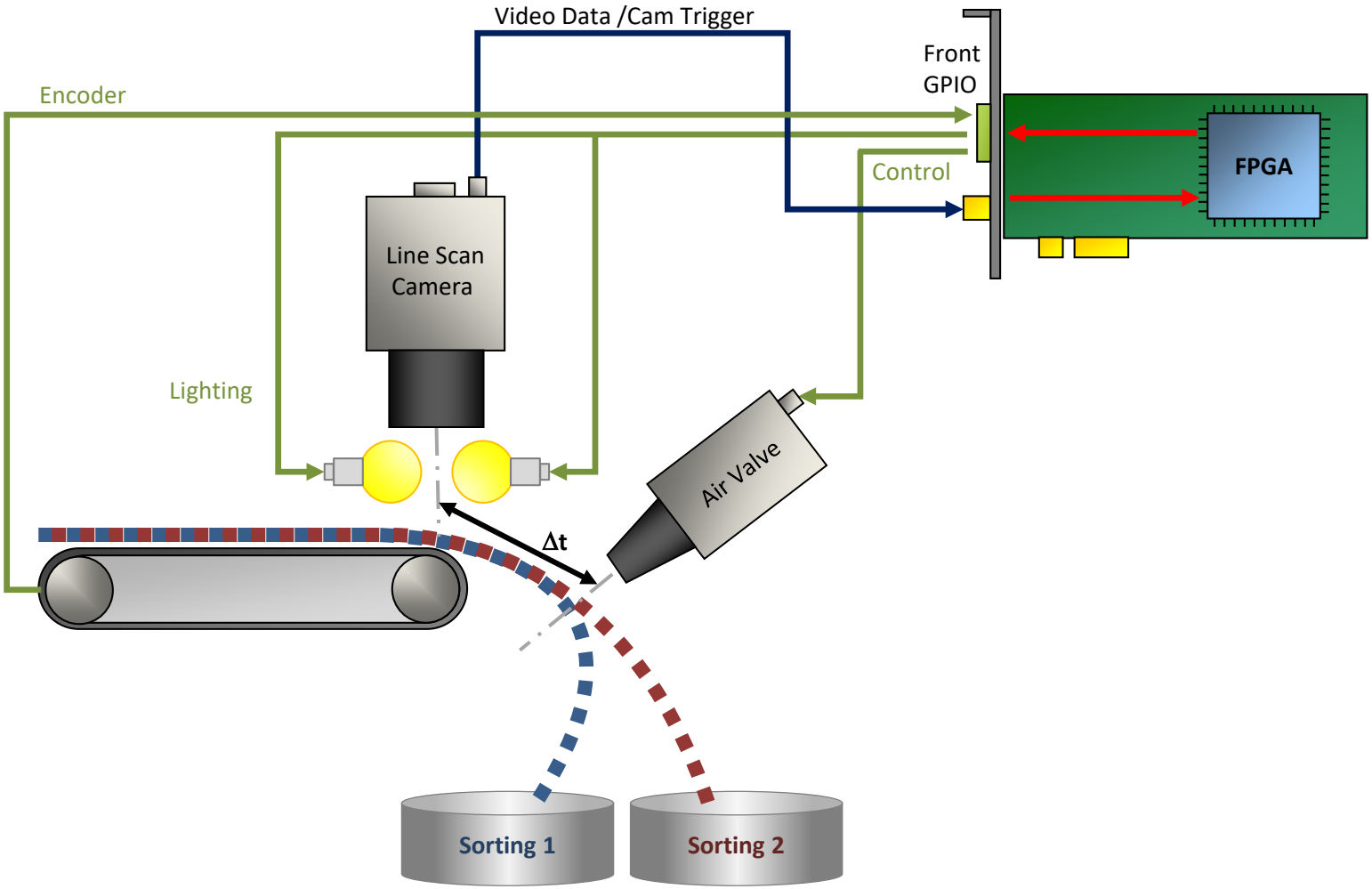
Trigger Front GPIO (Interface Card 1C)

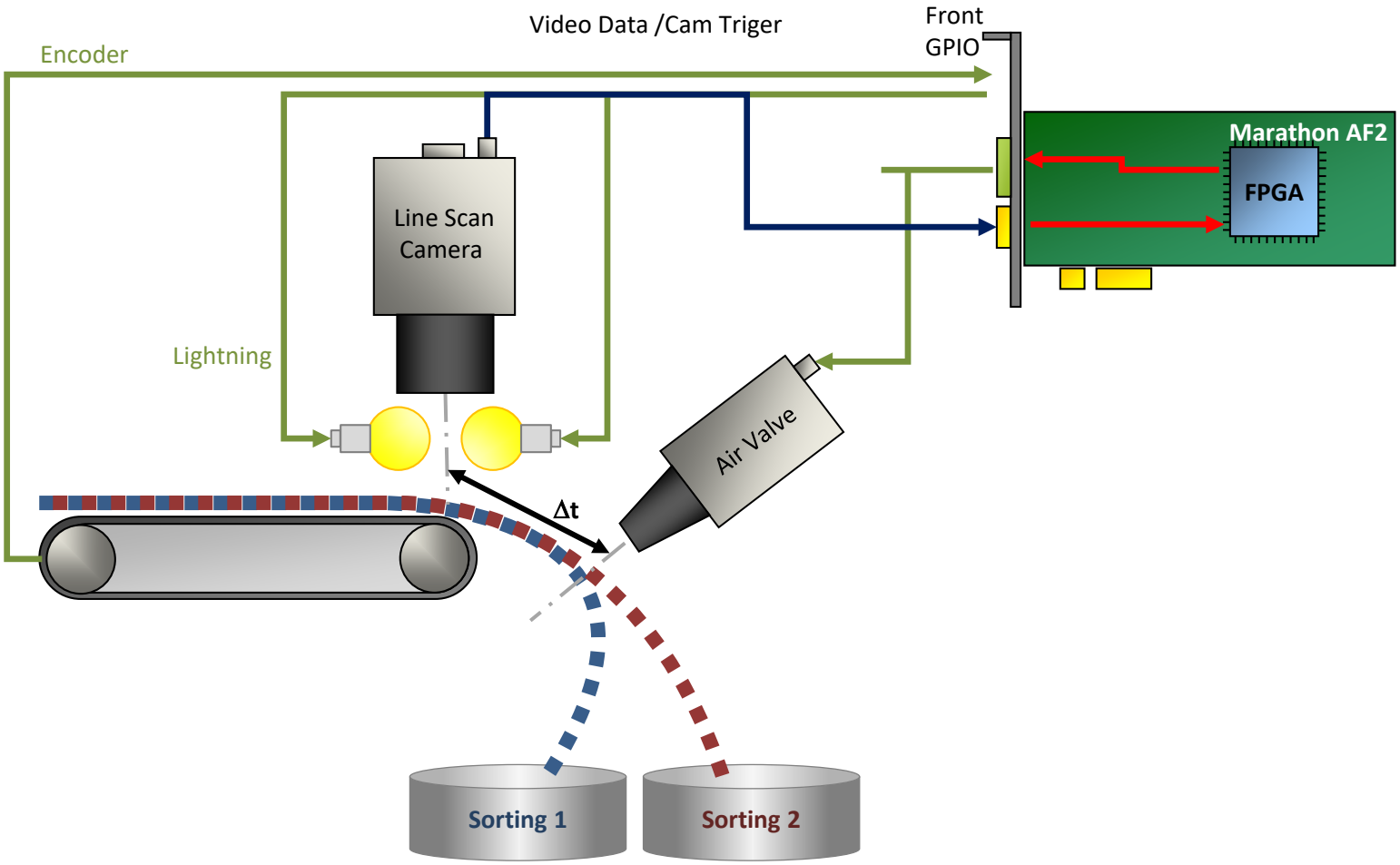



Encoder
Video Data /Cam Triger
Front
GPIO
GPIO
Marathon AF2
Control
FPGA
Line Scan
Camera
Lighting
Air Valve
Δt
Sorting 1
Sorting 2


Encoder
Video Data
Front
GPIO
CXP-12 Interface Card
Control
FPGA
Camera
Lighting
Air Valve
Δt
Sorting 1
Sorting 2

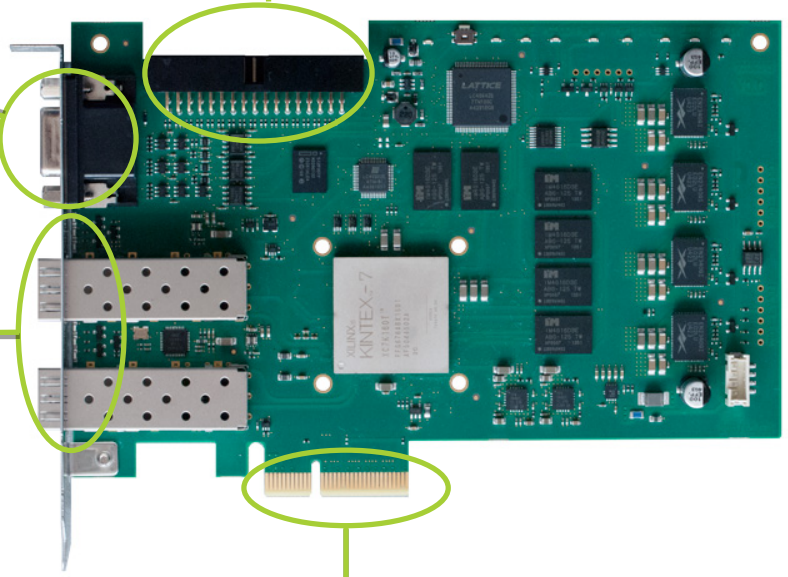
Interface Card 1C




Video Data /Cam Triger
Front
GPIO
Encoder
Marathon AF2
FPGA
Line Scan
Camera
Lightning
Air Valve
Δt
Sorting 1
Sorting 2

GPIO
Trigger board connection

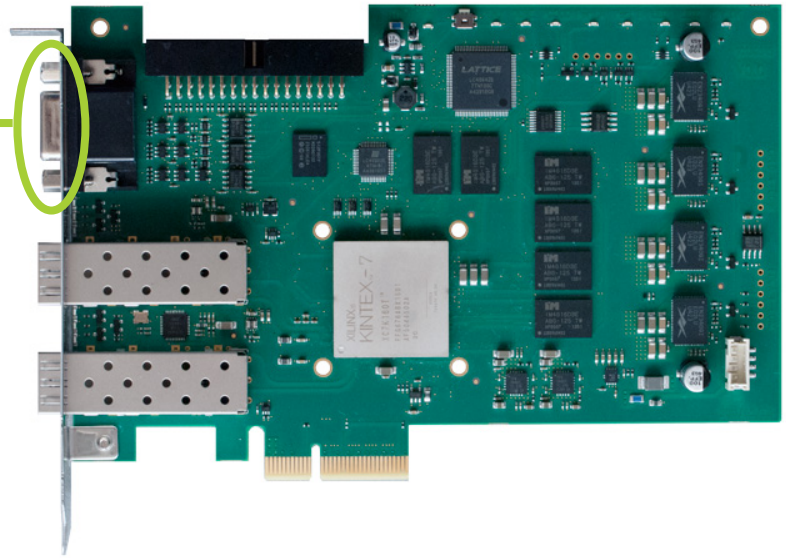
Front GPIO
Opto-coupled inputs TTL outputs, RS485, Shaft Encoder, Trigger

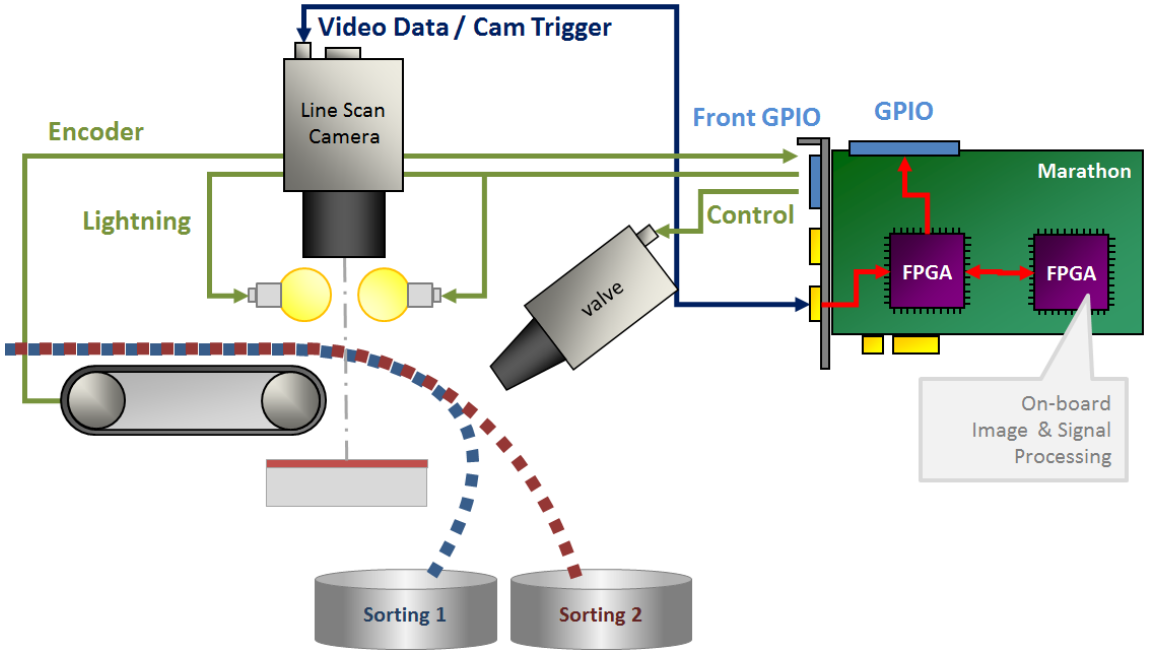


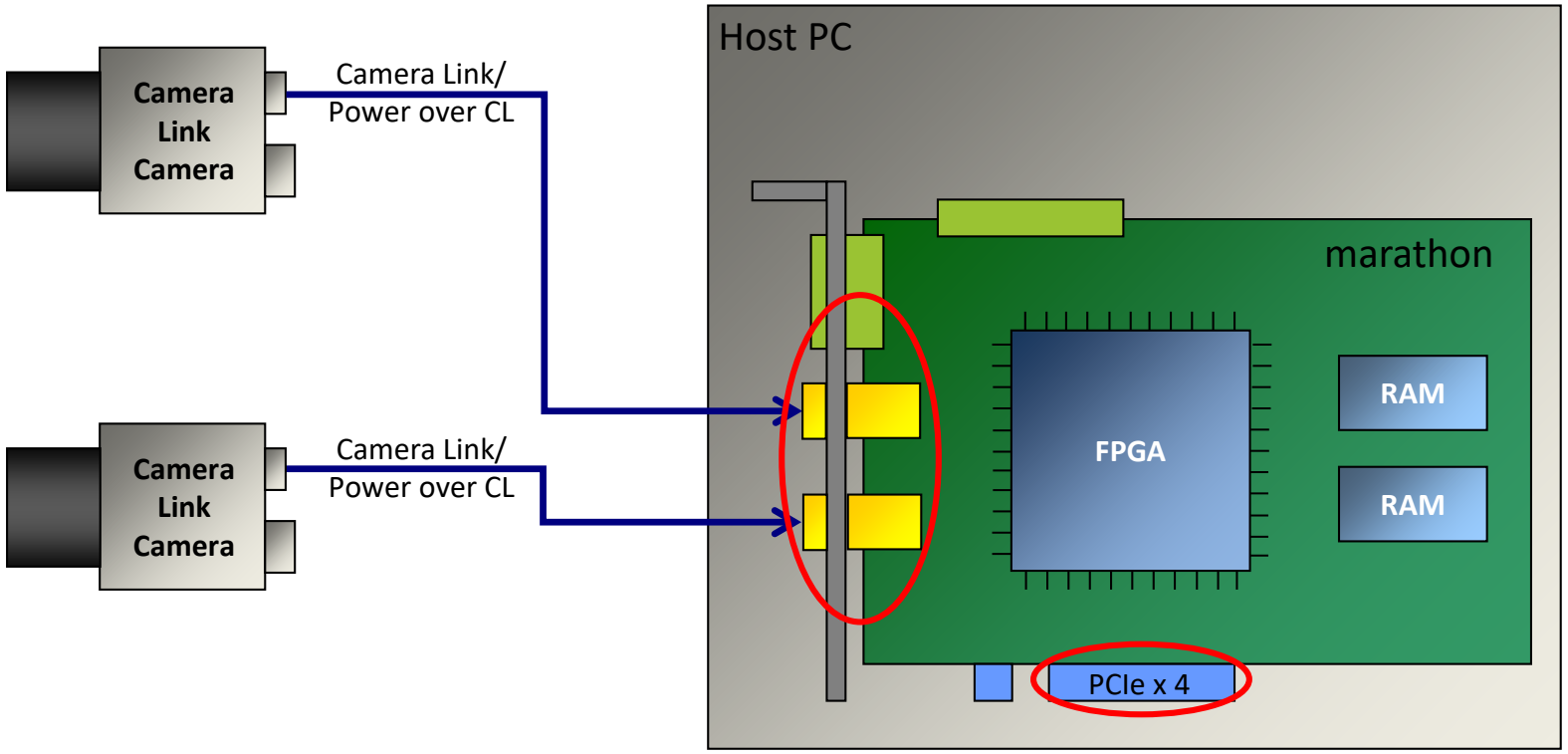
Camera Interfaces
SFP+ (10 Gbit)

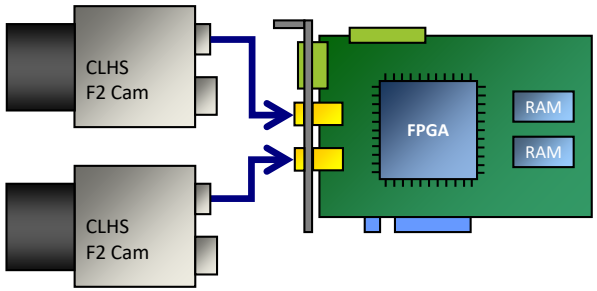
DMA1800 (PCIe x4 Gen2):
Up to 1.800 MByte/s

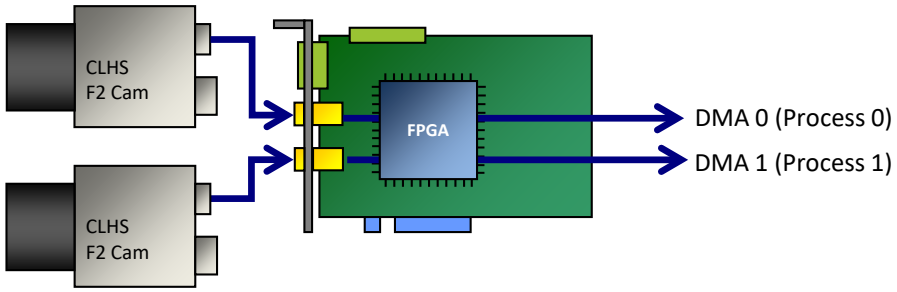
Front GPIO
Opto-coupled inputs,
TTL outputs

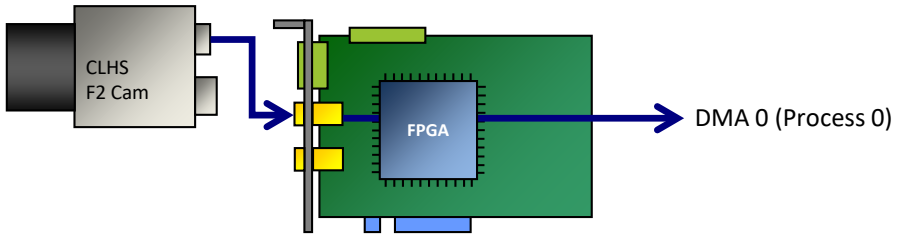



Video Data / Cam Trigger
Line Scan Camera
Encoder
Lightning
Front GPIO
GPIO
Marathon
Control
valve
FPGA
FPGA
On-board Image & Signal Processing
Sorting 1
Sorting 2


Camera
Link
Camera
Camera Link/
Power over CL
Camera
Link
Camera
Camera Link/
Power over CL
Host PC
marathon
FPGA
RAM
RAM
PCIe x 4

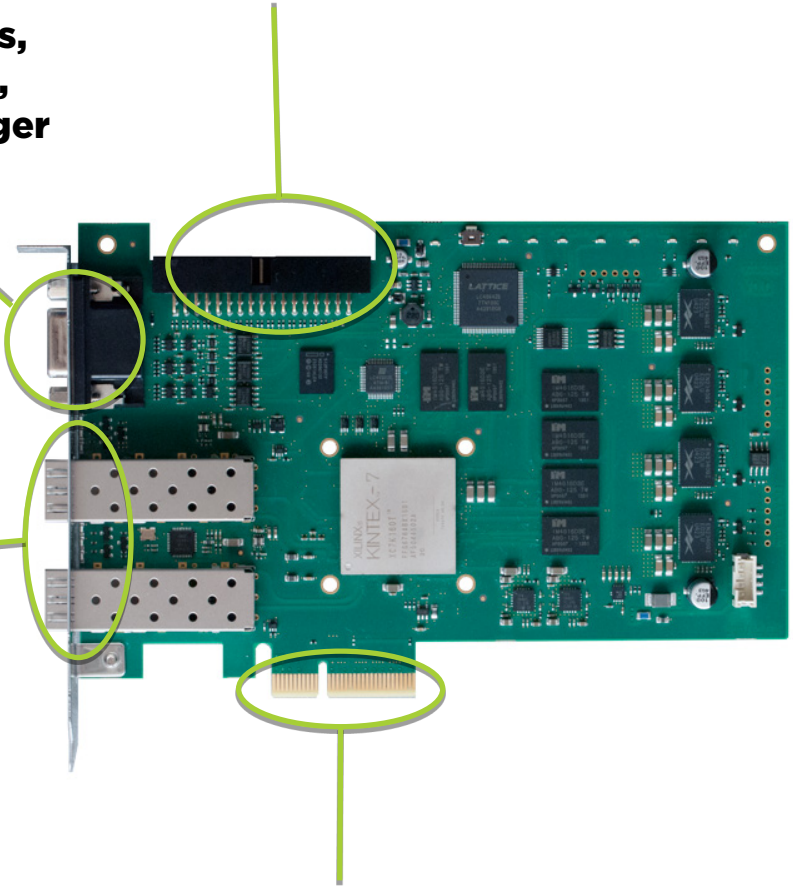

CLHS
F2 Cam
CLHS
F2 Cam
FPGA
RAM
RAM


CLHS
F2 Cam
CLHS
F2 Cam
FPGA
DMA 0 (Process 0)
DMA 1 (Process 1)


CLHS
F2 Cam
FPGA
DMA 0 (Process 0)

GPIO
Trigger board connection

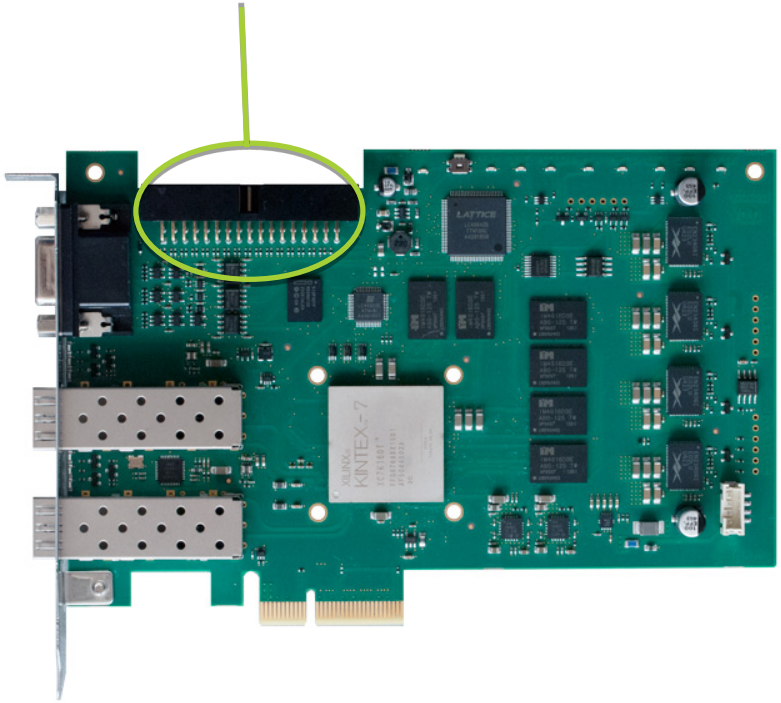
Front GPIO:
Opto-coupled inputs, TTL outputs, RS485, Shaft Encoder, Trigger



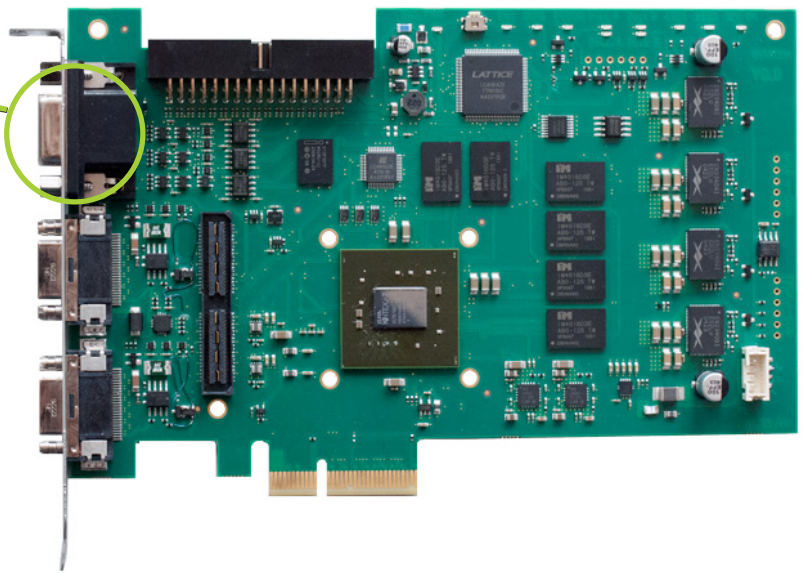
Camera Interfaces
SFP+ (10 Gbit)

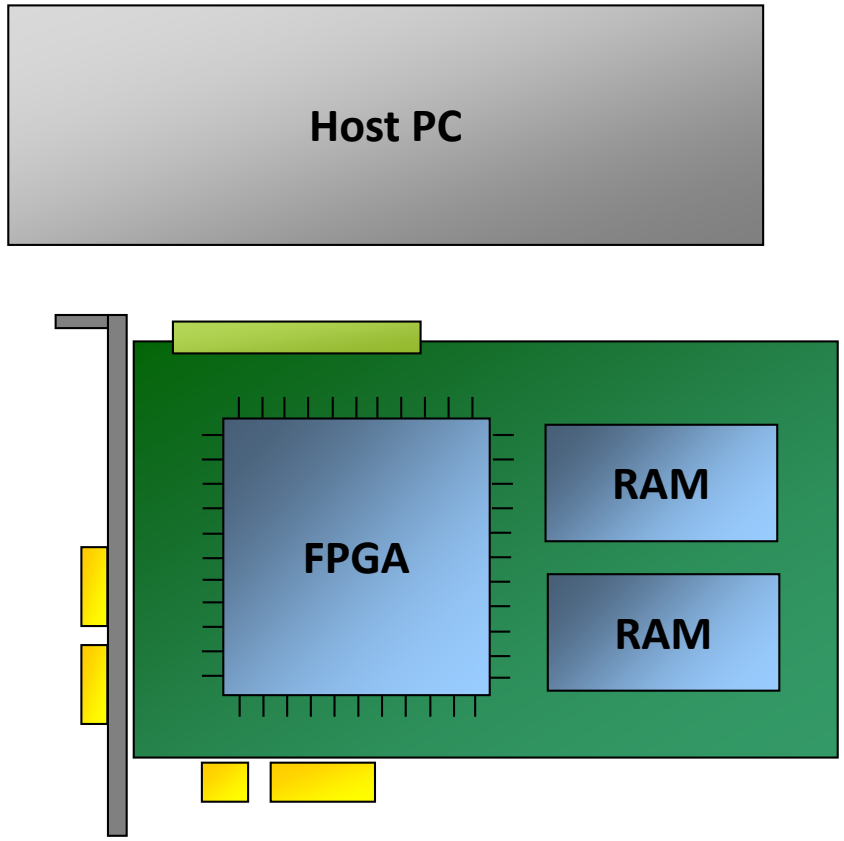
DMA1800 (PCIe x4 Gen2):
Up to 1.800 MByte/s

GPIO
Trigger board connection



Front GPIO:
Opto-coupled inputs
TTL outputs, RS485




Host PC
FPGA
RAM
RAM